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Applications of Signal Processing, Fast Algorithms and Multivariable Control to Semiconductor Manufacturing

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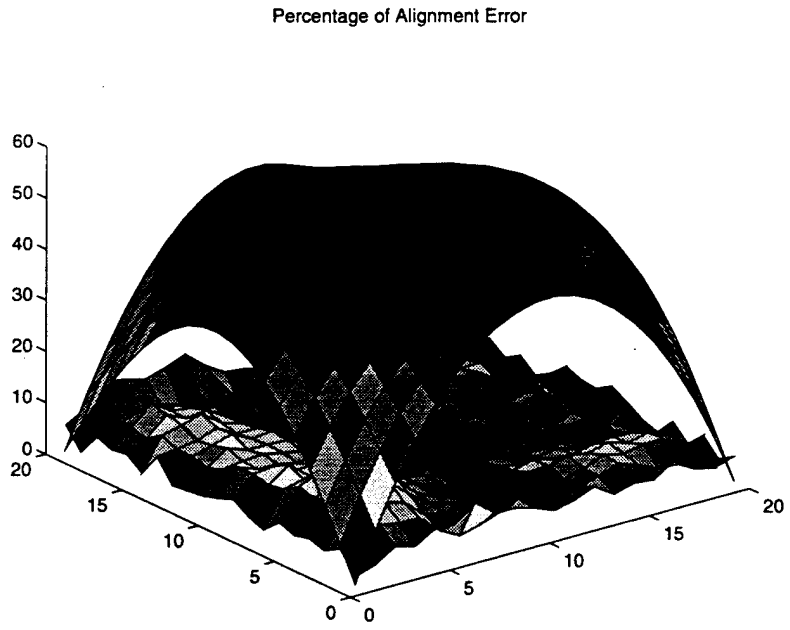

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1 Overview

The aim of this project was to demonstrate that a systems-based methodology, utilizing the tools of fast algorithms, signal processing, and multivariable control, can make a significant difference to the efficient solution of various critical problems in the fields of semiconductor manufacturing and materials processing. Specifically, the following developments were achieved:

1. A robust multivariable control algorithm for use in several types of rapid thermal processes including oxidation, annealing, and silicidation as well as single-wafer chemical vapor deposition processes,

2. Introduction of novel signal processing techniques into a recently proposed acoustics-based technique for noninvasive temperature measurement of RTP wafers,

3. Subspace-based image processing strategies for defect inspection of periodic patterns in patterned wafers, distortion compensation for accurate overlay in lithography of quasi-periodic patterns, circle and ellipse fitting, and critical dimension measurement,

4. Fast algorithms for the systematic design of phase-shifting masks.

In almost all cases, our algorithms were tested both in simulation and in actual implementation in an experimental or prototypical setting.

In the area of controls for rapid thermal processing (RTP), during 1992-1993, we successfully transferred our RTP control technology to Texas Instruments (Dallas, TX) where it was utilized during the 1,000 wafer demonstration of their Microelectronics Manufacturing Science and Technology (MMST) program of flexible single-wafer IC fabrication. The temperature control technology was subsequently licensed via MMST to CVC Products (Rochester, NY) where it is currently being integrated into their commercial RTP equipment.

This work has also been well received in the professional community. Our paper, "Model Identification in Rapid Thermal Processing Systems", by Y. Cho and T. Kailath, received the 1993 Best Paper Award by the IEEE Semiconductor Manufacturing Society. An invited review of our work is to appear in the *Control Handbook*, edited by W. Levine, CRC Press, 1996.

Further, the work and concepts of RTP were extended to problems in the thermal processing steps of bake and chill in the microlithography sequence. Here, we designed a new multizone system with a short thermal response time and dual baking and chilling characteristics

allowing for spatial control of temperature uniformity. The systems methodology of simulation, optimization, actuator and sensor placement, control design, implementation and field testing, played a critical role in the evolution of this unit. At each stage of the design phase, the effects of design alternatives on the impact of closed-loop control were analyzed. It was made clear that good designs for closed-loop control could be quite different from those for open-loop operation.

In the area of signal processing for smart sensing, we have developed techniques to determine a discretized distribution of wafer temperature based on a sensor under development in Ginzton Labs at Stanford which measures the "time-of-flight" of a Lamb wave traveling through a semiconductor wafer. This information is dependent on the integrated wafer temperature along the path between the "transmit" and "receive" ultrasonic pins that support the wafer. The signal processing issues that were resolved included the appropriate placement of the pins to maximize signal-to-noise and a model-based estimate of the wafer temperature distribution as opposed to the average temperature along the measurement path.

In addition, we have developed several new image processing techniques for wafer defect inspection, alignment and metrology. Earlier work involved the development of a new *Subspace-based line detection* (SLIDE) algorithm which, among other applications, was shown to be effective for detecting and estimating a set of parameters that can be used to mathematically model the patterned features on a wafer. With some modifications and enhancements, this algorithm was used to obtain a scheme for rapid inspection of regular patterned structures such as those found in DRAM memory cells and flat panel display (FPD) cells. This algorithm has been tested on a number of real patterned FPD images provided by Xerox PARC (Palo Alto).

In the area of phase-shifting mask design, we developed and tested a fast model-based systematic mask design algorithm. The algorithm is based on solutions to a classical image reconstruction problem. Both simulation and experimental results have successfully demonstrated designed phase-shifting masks for both simple patterns such as contact holes, gratings, and U-patterns, and more complex patterns such as SRAM and gate-array designs. The experimental testing was carried out in collaboration with Matsushita Corporation (Kyoto, Japan) and HP ULSI Research Laboratory (Palo Alto, CA). Also as a result of this work, a novel simulation model for projection lithography was developed. The aerial image simulation model is computationally more efficient than prior models.

Several Ph.D. theses were completed during this project: H. Aghajan, Y. Cho, C. Chang, P. Park, Y. Wang, and B. Khalaj. Two of the graduates are currently employed in the

semiconductor industry.

Considerable efforts were made to publish the results in the open literature (see sec. 7). Thirty papers have already appeared in leading journals; one of them obtained the 1993 Outstanding Paper Prize from the IEEE Transactions in Semiconductor Manufacturing (see App. A). Six more journal papers are to appear shortly and several more are in various stages of the refereeing process. Finally, more than 40 papers have been presented at various conferences and symposia.

In this final report, our work during 1993-1995 is summarized with an emphasis placed on work done in 1995. Additional summary material for 1993 and 1994 is contained in their respective annual reports. Comprehensive discussions can be found in the journal and conference papers, cited at the end of the report. Copies can be made available upon request, and sent electronically if desired.

2 Control of Thermal Processes

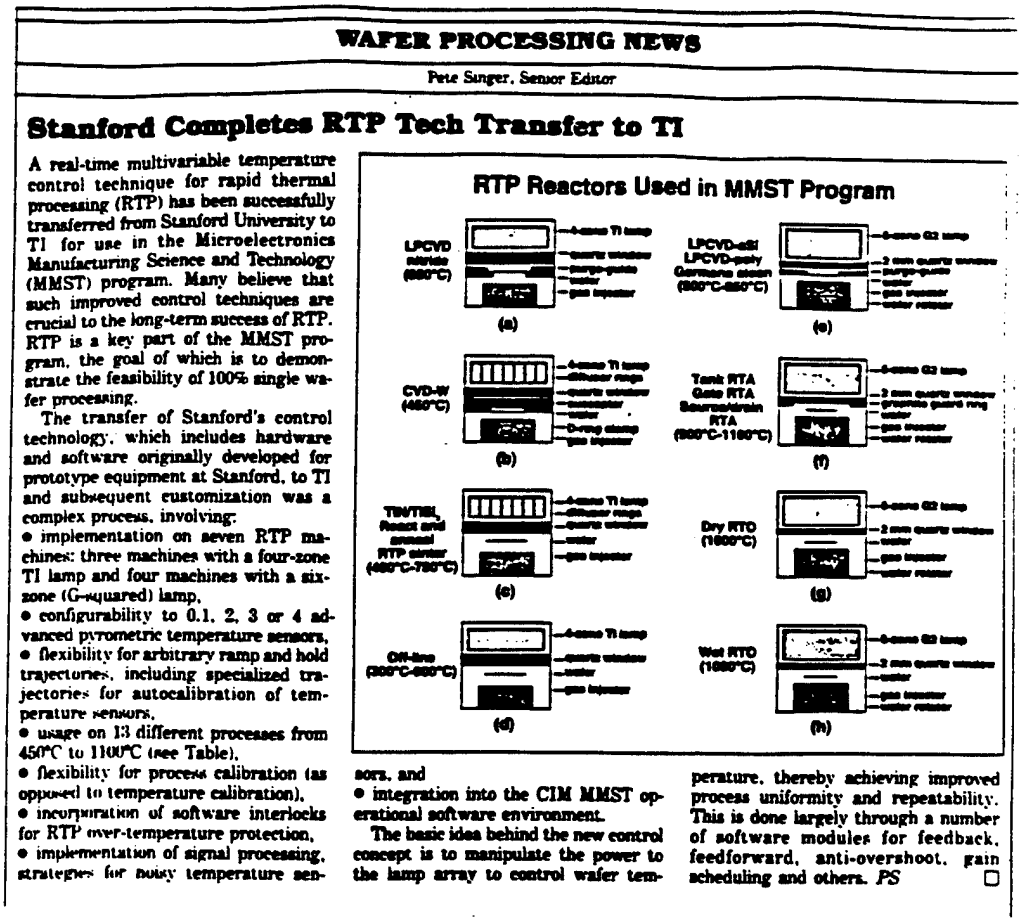
Our initial focus, starting in 1990 and continuing until 1994, was on multivariable temperature control for RTP systems. This effort has led to several Ph.D. theses, journal and conference publications, and successful technology transfer to industry. (see Sect. 2.1.)

In addition, based on our work in RTP, we have begun the development of novel technology and controllers for the thermal processing operations involved in the microlithography sequence. (see Sect. 2.2.)

2.1 Control of Rapid Thermal Processing (RTP)

In order for RTP to be a viable option for the production of integrated circuits, stringent Though RTP has been under study for nearly two decades, implementation had been delayed because of the difficulties in meeting the required transient and steady-state temperature uniformity specifications. One approach to achieve this objective is to utilize a multizone radiative lamp that provides an energy flux with the proper distribution over time to maintain uniformity. (Incidentally, the conventional wisdom till we began our studies was that somehow a *uniform* flux distrubtion over the wafer had to be achieved. Our mathematical analysis showed that such a uniform flux distribution would never yield a satisfactorily uniform temperature distribution.) In order to achieve this automatically and precisely, a real-time control algorithm must be devised. In this project, several multivariable control strategies were developed and tested. To design the controller, a systems-based methdology was used that involved the investigation of a number of topics including: (1) Determining the performance limits of RTP through the use of optimization techniques, (2) Developing model identification strategies for control and sensing, (3) Designing and implementing advanced control strategies, (4) Developing discrete event control strategies for recipe synthesis and control. All these issues and several others, arose in the design of a multivariable temperature control strategy that was demonstrated on a prototype 3-zone system at Stanford. Subsequently, this strategy was transferred to Texas Instruments and demonstrated within their MMST program. The original Stanford controller designed on a simple university research chamber was extended to work with different chambers and 13 different processes (see Fig. 1). The control technology, with some modifications, is currently being used in a commercially available RTP system from CVC Products.

A tutorial report on our work can be found in the invited paper [1].



WAFER PROCESSING NEWS

Pete Singer, Senior Editor

Stanford Completes RTP Tech Transfer to TI

A real-time multivariable temperature control technique for rapid thermal processing (RTP) has been successfully transferred from Stanford University to TI for use in the Microelectronics Manufacturing Science and Technology (MMST) program. Many believe that such improved control techniques are crucial to the long-term success of RTP. RTP is a key part of the MMST program, the goal of which is to demonstrate the feasibility of 100% single wafer processing.

The transfer of Stanford's control technology, which includes hardware and software originally developed for prototype equipment at Stanford, to TI and subsequent customization was a complex process, involving:

- implementation on seven RTP machines: three machines with a four-zone TI lamp and four machines with a six-zone (G-squared) lamp,
- configurability to 0.1, 2, 3 or 4 advanced pyrometric temperature sensors,
- flexibility for arbitrary ramp and hold trajectories, including specialized trajectories for autocalibration of temperature sensors,
- usage on 13 different processes from 450°C to 1100°C (see Table),
- flexibility for process calibration (as opposed to temperature calibration),
- incorporation of software interlocks for RTP over-temperature protection,
- implementation of signal processing strategies for noisy temperature sensors, and
- integration into the CIM MMST operational software environment.

The basic idea behind the new control concept is to manipulate the power to the lamp array to control wafer temperature, thereby achieving improved process uniformity and repeatability. This is done largely through a number of software modules for feedback, feedforward, anti-overshoot, gain scheduling and others. *PS* □

RTP Reactors Used in MMST Program

Figure 1: Schematic of temperature controlled RTP chambers used during MMST at Texas Instruments. From P. Singer, *Semiconductor International*, Vol. 16, No. 7, pg. 58, June 1993.

2.2 Thermal control of microlithography baking

Thermal processes are an essential ingredient of microlithography. Semiconductor wafers typically undergo soft bake and post exposure bake steps, and often other baking steps (depending upon the process) during lithography. Increased throughput and better wafer temperature uniformity during bake are critical to improving the bake step. A variety of mathematical models can be used to study the effects of various influences and help identify limitations of current designs. In particular, one-dimensional dynamic modeling of heat transfer from a bakeplate to a wafer is useful in understanding transient behavior, which affects both the throughput and uniformity.

Current approaches to baking employ a plate with a large thermal mass maintained at a near constant processing temperature. The plate contains embedded pins which support a wafer slightly elevated above the plate. This is called "proximity heating". A cold wafer is dropped onto the plate, which then rises to the processing temperature. A one-dimensional

discrete time model of the process can be shown to be of the simple form

$$T_w(n) = aT_w(n-1) + bT_p,$$

where T_w is the wafer temperature and T_c the plate temperature. Figure 2 shows the results for identifying this model given experimental step response data.

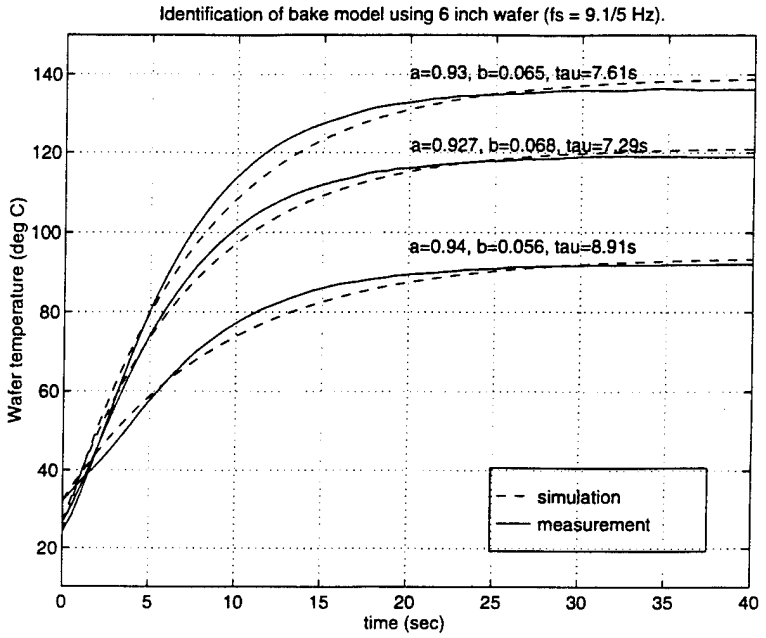


Figure 2: Measured and simulated wafer temperature responses used in identifying model parameters.

This model has been extended to two dimensions in order to study uniformity effects. Our ultimate objective is to develop a bake system that can achieve fast ramps and good spatial control of wafer temperature. There are several challenges to achieving this objective, including design of the wafer heating mechanism, sensing of the wafer temperature, and control of the wafer temperature in real-time.

Our efforts have been targeted towards the use of an array of thermoelectric elements that serve a dual purpose of heating and cooling. In this manner, we should be able to demonstrate both baking and chilling for microlithograhpy within the same unit. We have begun to construct an experimental apparatus to test out our model predictions.

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Saraswat, M. Moslehi, and C. Davis, "Control for Advanced Semiconductor Manufacturing: A Case History," Chapter 73 in *The Control Handbook*, W. Levine, ed., pp. 471-487, CRC Press, 1996.

3 Signal Processing for Smart Sensing

Precise wafer temperature measurement and control are crucial to the viability of rapid thermal processing (RTP) technology for semiconductor manufacturing. In this project we examine the problem of accurate noninvasive measurement of wafer temperature, which is required for precise temperature control. Experimentation and simulation studies have successfully demonstrated that *smart* temperature sensors equipped with modern signal processing techniques can provide new possibilities for temperature measurement and also for other sensing problems. Moreover, fast and powerful computer chips can be readily employed to enhance existing sensor technology without requiring costly hardware additions or modifications.

This section of the report is ordered chronologically. It expands upon the following accomplishments: (1) Recognition of the limitations of existing technologies of pyrometry and thermocouples, (2) Investigation of ultrasonic sensing technology, (3) Designing and debugging of a new system for RTP, (4) Multivariable control in RTP using ultrasonics, (5) Application of sensing to Flat Panel Display technology.

3.1 Limitations of existing pyrometry and thermocouple technology

Pyrometry, the most commonly encountered temperature sensing technique used in RTP suffers from large bias due to uncertainty in the emissivity of silicon wafers, arising chiefly from changes due to oxide growth. Texas Instruments recently proposed an innovative technique to reduce this problem by placing the pyrometers on the same side of the silicon wafer as the lamps. Processing takes place on the other side, so that the emissivity properties of the reverse side should be relatively unaffected, except by temperature. However this solution in turn brings up a new problem. Typically, conventional pyrometers cannot distinguish between the radiation components from the lamp and from the wafer. Thus, the pyrometer temperature readings will be higher than the actual wafer temperatures. We developed an adaptive technique to cancel the lamplight interference by exploiting differences in the the primary frequency components of the two radiative sources[3]. The wafer radiation has a relatively low frequency spectrum (less than 10 Hz), while the lamp intensity can be modulated much more rapidly (at 30 Hz for implementation reasons). Our lamplight elimination scheme detects the modulation intensity and removes from the total received signal a value proportional to the detected modulation intensity. The algorithm has been tested with real data and is shown to perform well. It has been successfully used in several rapid thermal

processing machines, executing many different processing steps.

Investigations of embedded thermocouple wafers reveal several interesting results [4]. Embedded thermocouple wafers are typically made with all of the thermocouples embedded on the same side of the wafer. In RTP reactors which use single sided heating, the measured temperature when the thermocouples (junctions, wiring, bonding material, etc.) face the lamps versus face away from the lamps can be dramatically different. For example, at 1000 °C the difference was measured to be 54 °C . Because of silicon's relatively high coefficient of thermal conductivity, the temperature difference between the wafer's front and backside has been estimated to be on the order of 4 °C in single sided heating reactors. See Figure 3. Experiments growing oxide in both configurations show negligible differences between the two configurations. This suggests that the *thermocouple readings* are in error and lead to a special calibration procedure.

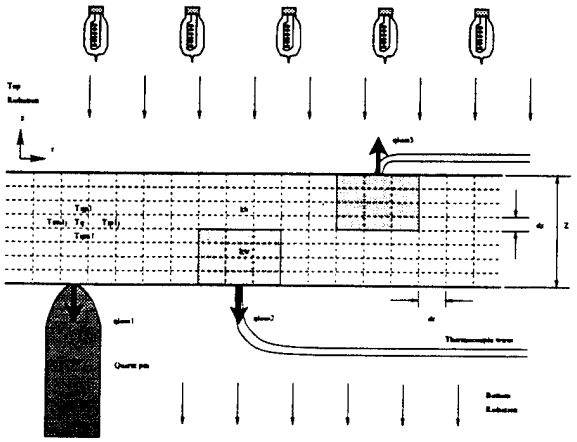

Figure 3: At 1 atm ambient and approximately 1000 °C and with the thermocouples facing the lamp, typically a 50 °C hotter reading is obtained. This is fairly amazing because the axial distribution is not expected to exceed 4 °C .

Several possible sources for the error exist. Thermal modelling predicts that *local* thermal losses caused by both the wiring and the bonding material which attachs the thermocouple junction to the wafer can produce errors on the order of magnitude observed above. This has led a prominent industrial partner, SensArray. Corp. (Santa Clara, CA), to change how the embedding currently takes place.

3:2 Ultrasonic sensing technology

Researchers in Stanford's Ginzton Laboratory, specifically B.T. Khuri-Yakub and his students, inspired the work on the use of the ultrasonic sensors [2]. The idea is that the velocity of a travelling acoustic wave through a thin plate (*i.e.*, a silicon wafer) depends upon the bulk temperature. By measuring the time of flight (TOF) and knowing the distance between the transmitter and the receiver, the average velocity along the path can be measured. Then, the measurements can be used via a tomographic inversion technique into an estimate of the spatial temperature distribution. Figure 4 conceptually illustrates the measurement setup.

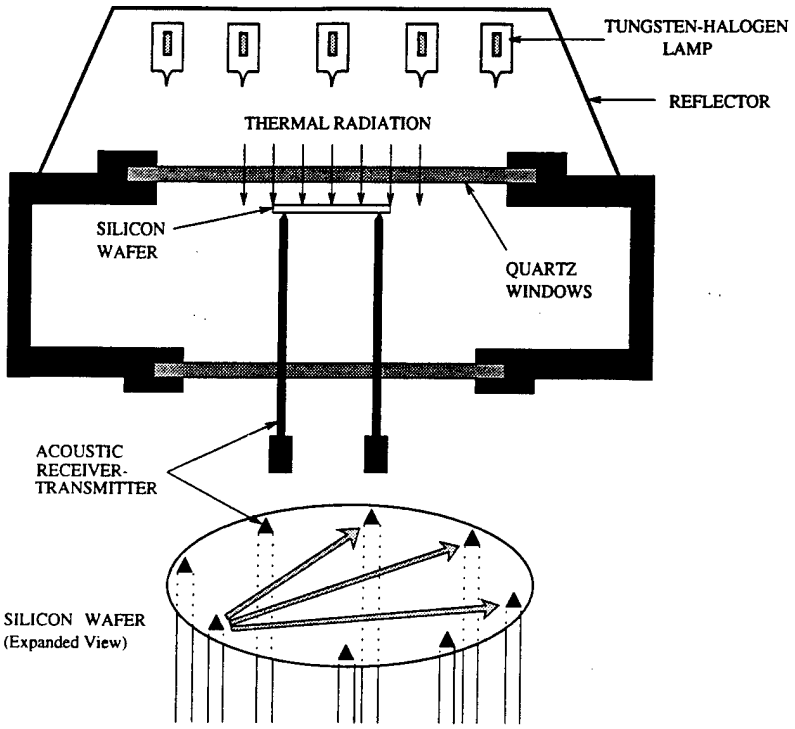

Figure 4: A typical cross-section of a Rapid Thermal Processor (RTP) using an acoustic thermometry system.

Clearly, a number of modelling assumptions need to be made to reconstruct the entire spatial temperature profile from a limited number of measurements. Hence, there are a number of methods that can be considered. These vary the sizes and shapes of the pixels used in a discrete approximation to the continuous temperature profile. Square and annular pixels are the most natural methods to consider. These result in a least squares problems.

An alternative approach is a regularized tomographic inversion technique to estimate wafer temperature from time of flight measurements of acoustic waves in silicon. A regularizing functional is designed to incorporate *a priori* knowledge of properties of the tempera-

ture distribution and serves to stabilize the temperature estimation process even when the number of available sensors is reduced. Simulation studies showed that our technique can solve several potential problems of existing methods and give improved estimates of temperature profiles [5]. These methods are easily modified in the case of sensor failure and/or degradation.

3.3 Designing and debugging of a new system for RTP

An experimental RTP system in Stanford's Center for Integrated Systems was adapted for the newly designed ultrasonic sensors.

As with any experimental system, there are a large number of design decisions which need to be made in order to achieve a working system. These include selection from among the different types of acoustic waves that the quartz pins and the silicon wafer will support, designing the quartz pins to increase the coupling of acoustic energy into the wafer, and hardware design. Problems with both coupling of acoustic energy through the cooling water and the high temperatures were destroying the vacuum seal were remedied. The development work has lead to improved understanding of many of the practical issues involved and generated ideas for future designs both in RTP systems as well as for other semiconductor manufacturing tools (*e.g.* sputtering and plasma etching system).

One of the most important factors is maintaining a fixed contact distance between transmitter and receiver pins. Long support pins can lead to undesirable flexibility and discontinuous jumps in the data. Related systems designed with this insight have achieved repeatable contact.

The three pin sensor plate designed was optimized in the sense of minimizing the condition number of the matrix which maps time of flight into temperature. The solution to the original formulation as an unconstrained minimization problem places two of the three sensor directly across from one another on the wafer. This configuration is unstable in the sense that the wafer will not be balanced; equivalently one of the contact forces goes to zero. To overcome this difficulty, the problem was reformulated as a constrained minimization problem. The constraint is that the contact force between the wafer and the pin must be greater than some normalized threshold value. Sufficient contact force also assures that Hertzian contact will provide enough energy coupling between the quartz pins and the wafer. Figure 5 shows a tradeoff curve for condition number versus the contact force.

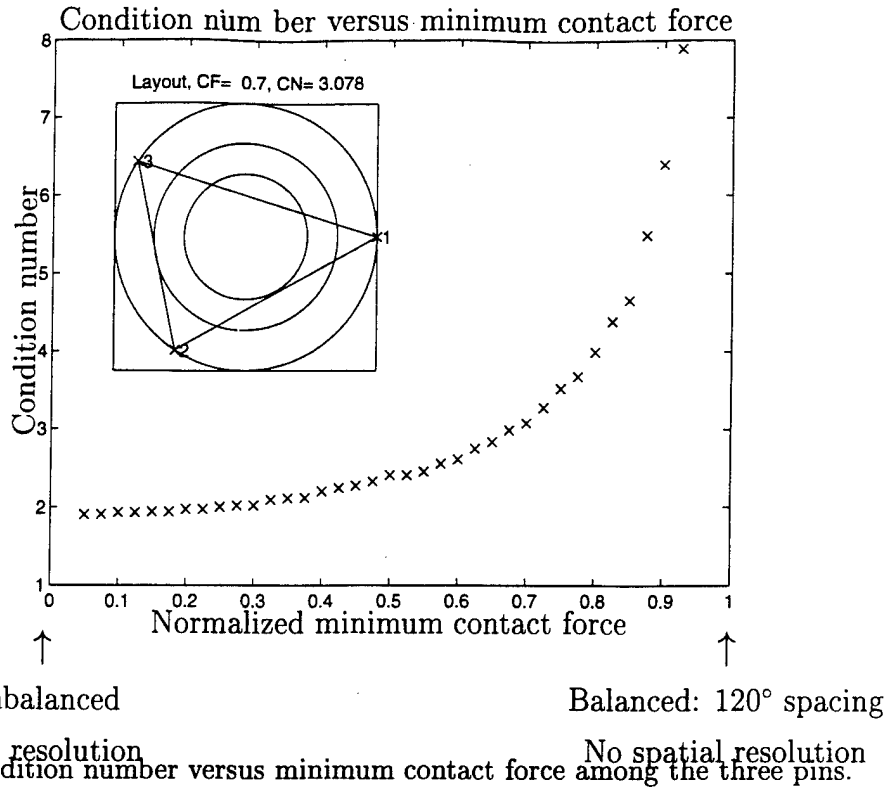

Figure 5: Condition number versus minimum contact force among the three pins.

3.4 Multivariable control in RTP using ultrasonics.

Using the ultrasonic sensors, it is possible to design a multi-input, multi-output controller for the RTP system. A more detailed discussion of the modelling, controller and the appropriate sensing conditions can be found in [8].

Modelling was done using the ESPRIT algorithm and an LQG controller was designed around a particular operating point. The controller takes TOF readings as inputs and changes the lamp powers. The setpoints used by the TOF controller are determined by a calibration procedure involving a thermocouple wafer. TOF steps of 50 °C are shown in Figure 6. The average temperature along both paths is successfully controlled.

3.5 Application of sensing to Flat Panel Display technology.

Crystallization of thin Si/SiGe films for use in thin film transistors (TFTs) using rapid thermal annealing (RTA) offers great promise to the flat panel display industry. Temperature is commonly measured using pyrometry, which infers temperature from emissivity. Thus, this technique is eminently unsuitable for crystallizing films, which undergo rapid changes in emissivity due to phase changes. Also, no simple means of in-situ monitoring of film crystallinity exists.

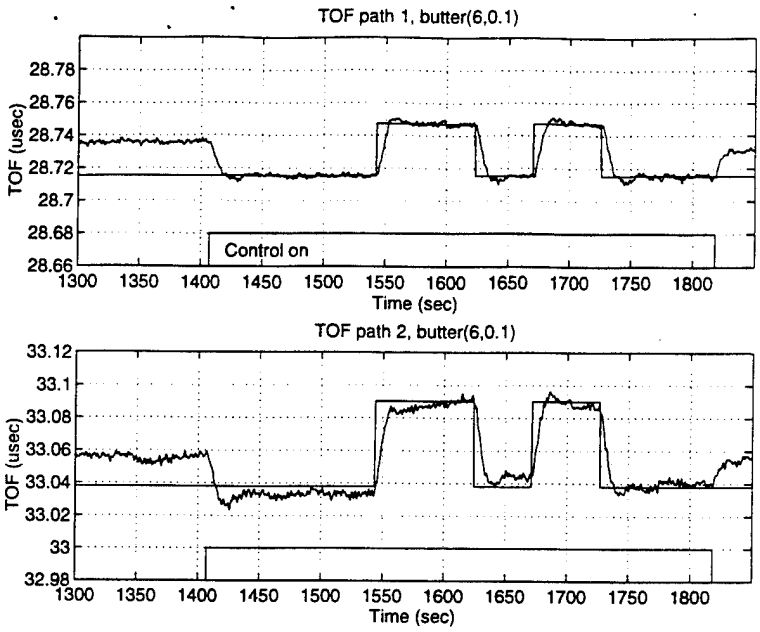

Figure 6: The TOF steps corresponding to 50 °C steps in temperature. A 6th order Butterworth filter with cutoff frequency of 0.5 Hz used to smooth data. The "Control on" line indicates when the closed-loop control is applied.

The ultrasonic sensors are being used to monitor crystal growth during processing. The time of flight readings are a strong function of temperature but independent of emissivity. Heat absorption by the substrate in an RTA is a function of film emissivity, and hence, of crystallinity. By isolating temperature from emissivity, it is possible to track crystallinity. Our results have established that TOF is suitable for determining crystallization end-points, and is also sensitive enough to identify the onset of crystallization prior to any visible change in film transparency.

This novel tool for determining film crystallinity and temperature simultaneously provides a means of minimizing thermal budgets and also modelling crystallization processes. Further details can be found in [9].

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4 Image Processing for Inspection, Metrology and Alignment

In this section, we report on our continuing work in the area of image processing for integrated circuit manufacturing applications. The objective of this work is to develop new image processing algorithms for defect inspection, wafer metrology and alignment. These areas of integrated circuit manufacturing technology currently rely heavily on the visual inspection and the intervention of human operators. Our motivation was to try to replace the manual (*e.g.* visual) inspection and alignment techniques by advanced image processing algorithms, which will not only improve the throughput by speeding up the processing, but also improve the reliability of the procedures.

Previously reported work discussed: (1) Inspection of patterned wafers for defects, (2) Estimating wafer pattern distortions to improve overlay accuracy during exposure, (3) Improved detection and measurement of features on the wafer for metrology and alignment. Our work in the third area mentioned above improves the performance of our previously-reported subspace based line detection (*SLIDE*) algorithm. In this section, we describe our recent efforts on distortion compensation for accurate overlay and on pattern assisted alignment techniques.

4.1 Distortion Compensation for Accurate overlay in Lithography of Quasi-Periodic Patterns

Alignment is the part of the lithography process concerned with positioning a wafer so that a new pattern can be exposed on the wafer in the correct position. As the minimum feature size of ICs decreases there is a decrease in the maximum alignment error that can occur before circuit malfunction. Therefore alignment algorithms of high accuracy are required. However, decreasing circuit size is also making lithography systems more expensive and therefore high throughput is another concern for modern lithography systems. In this work, we will present algorithms that are aimed at providing reasonable compromises between accuracy and throughput.

In general, the circuit has a minimum feature size, λ, and the alignment error must be kept below a fraction of λ in order for the circuit to operate within specifications. The maximum allowed overlay error is often assumed to be either 30% of λ, or 25% of λ. The actual accuracy required depends on the circuit complexity and how robust the circuit is

to parameter changes. As the complexity of circuits increases the required accuracy will increase as well. The accuracy of the alignment process also has a significant effect on the yield of the process, where yield is defined to be the percentage of ICs produced that operate within specifications. As the required alignment accuracy increases it would be expected that the time taken to align a wafer will increase, as more data will have to be processed to produce the required accuracy.

Lithography systems are very expensive, costing upto $4 million at 1992 with their cost rising exponentially and expected to reach $6 million by 1996. While the cost of lithography systems is increasing rapidly, the cost of computer processing is becoming cheaper and is now insignificant compared to the overall cost of the lithography system. It is therefore reasonable to expect that a large amount of computational power could be made available for alignment at a relatively small cost.

Often, magnification differences between mask and wafer dominate the distortion. These may arise from differences in temperature between when the mask or wafer was patterned and when it is used or from wafer stress arising from processing steps. Nonlinear in-plane distortions can be minimized by careful wafer processing and by ensuring that both mask and wafer are held flat in their chucks. The distortion introduced by some manufacturing steps on wafers can sometimes have a strong effect on overlay results. Thermal processes, for example, can introduce wafer distortions that can not be completely compensated by the stepper alignment system with a consequent degradation in overlay.

The effects of substrate distortion on overlay accuracy are much more pronounced when considering large substrates, such as for flat panel displays. Unlike conventional IC processing, thermal processing of glass substrates above 350^o C may induce glass compaction of as much as 100 ppm. To align to each process layer below, the stitching aligner must compensate for thermally induced plate size changes. Small errors in image placement or alignment may cause visible artifacts in the finished display.

At every step of the process of lithography, new mask patterns must be accurately aligned with previous patterns on the wafer surface. Wafer alignment is done by two basic means, either remote from the projection lens (global) or through the projection lens (local alignment). 'Global' alignment is carried out by aligning at a few sites (at least two) per wafer and then stepping the stage and exposing the entire array of sites using laser interferometers to monitor stage position. 'Local' alignment requires aligning the mask to the wafer after stepping to each new field before exposure. In general, alignment at each field of an step-and repeat camera provides the best overlay accuracy in optical lithography. However, global

alignment is primarily used on all but the most critical of alignment levels. This is due to much higher throughput that global alignment allows. Present practice in most cases is to use global alignment to save time, as the total time for stepping, alignment and exposure is generally required to be about one second.

As discussed earlier, in general, the repeated structures on a patterned wafer, are somehow shifted from their desired position on a rectangular grid. The primary contributors to substrate distortion in lithography are substrate warpage and thermally induced distortion, magnification errors and process induced distortion. In these situations, to obtain a very accurate site-by-site overlay, it is necessary to estimate the amount of misalignment of each cell beforehand. Computing the two-dimensional cross-correlation of the input image with the image of a defect-free cell gives a good estimate of the location of each cell, but it is computationally demanding. In this work, we have shown that global alignment combined with timely and accurate estimates of substrate distortion can provide greatly improved overlay accuracy with very modest increases in overall processing time. The proposed technique first estimates the distortion throughout the wafer and then uses the estimated distortion function to interpolate between global alignment sites. Our distortion estimation step is based on the fast signal processing technique for accurately estimating the distortion function of patterned wafers with quasi-periodic patterns described in our earlier work [2]. The method described, reduces the problem of estimating the two-dimensional distortion function to a sequence of one-dimensional problems and thereby affords substantial computational savings over alternative methods that involve computing two-dimensional cross-correlation functions.

Our approach may be summarized as consisting of the following steps (see also Figures 7 and 8):

1. Estimating the distortion function over the entire substrate after processing each layer
2. Using global alignment to align the image of next layer to the previous one at a few check points
3. Using the estimated distortion function to *interpolate* between alignment sites *i.e.* to predict the location of intermediate cells and compensate for the misalignment accordingly.

In the first step, the horizontal and vertical misalignment of each individual cell is estimated separately by projecting each row and column of the cells in both directions [2].

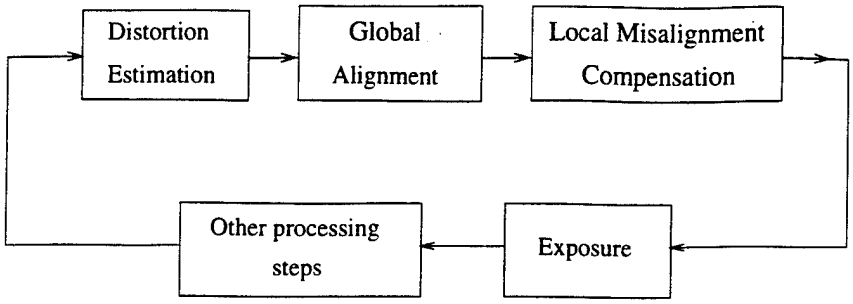

Figure 7: Diagram of distortion compensation scheme

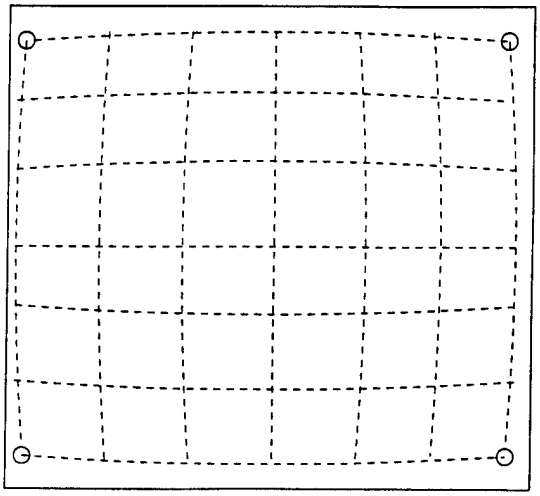

Figure 8: Location of global alignment marks and distortion pattern in the wafer

After obtaining good estimates of the location of all cells in the image, global alignment schemes are used at a few points to provide a reference for the new mask to be exposed. The estimated misalignment of each cell is then used in the final step to compensate for the existing distortion.

To evaluate the performance of our proposed approach in contrast with global alignment schemes, we have considered a quasi-periodic pattern with some low-order distortions in the regular structure. The results of estimating the amount of misalignment of each cell is examined for both the proposed method and the method that only uses global alignment at a few checkpoints. The global alignment method that we used for comparison uses four points at the corners for aligning the patterns. After this alignment step, it uses linear interpolation to estimate location of other cells in the image. In Figure 9, the true location of the cells in the image and the corresponding estimated locations by the two aforementioned methods is shown. As can be easily verified, the proposed method provides better accuracy than the case

where only global alignment schemes are used. In addition, as was mentioned earlier, the amount of computations required for this proposed algorithm is much less than site-by-site local alignment schemes.

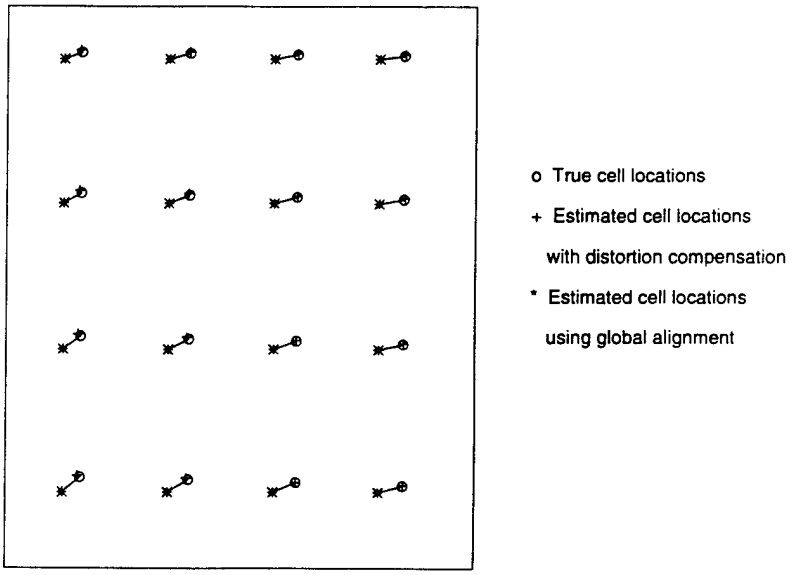

Figure 9: True and estimated cell locations: 'o' True locations; '+' Estimated locations using the proposed method; '*' Estimated locations using interpolated global alignment scheme.

4.2 Pattern-Assisted Alignment Technique

In the previous section, we introduced a new scheme for improving the performance of global alignment techniques in lithography of quasi-periodic patterns with low-order distortion, by estimating the distortion in the substrate. In this part, we show that the performance of site-by-site alignment techniques can also be improved by exploiting the structure of the patterns on the substrate and using them in combination with standard marks on the wafer. Our approach is based on the fast signal processing techniques for estimating the location and period of quasi-periodic patterns as discussed in our earlier work [1, 2].

The proposed pattern-assisted algorithm is based on improving the performance of site-by-site alignment scheme by incorporation of local pattern information. In standard site-by-site alignment techniques a mark at the boundary of each die is used for local alignment at that specific location of the wafer. In this work, the use of the patterns on the die instead of alignment mark is investigated.

In general, use of the pattern provides a series of advantages over use of standard marks

on the wafer. First of all, the pattern constitutes more information than typical alignment marks and this information can be fully exploited by incorporating the pattern structure in alignment. An important factor in accuracy of alignment techniques is the performance of estimating the position of pulses in the signal. The performance of the pulse location estimation techniques in turn depends on the number of edges in the signal, of which there are more in typical patterns than the number in standard alignment marks. Another important advantage in use of patterns for alignment versus marks is the fact that the ultimate goal of an alignment process is aligning the pattern, not the alignment mark. Due to distortion, the relative location of marks and patterns might change in between different processes. Therefore, aligning patterns reduces overlay variance by almost a factor of two compared to mark-based alignments. In addition, by keeping track of the periods of patterns exposed on the wafer, the scaling misadjustments in between steps can be identified and compensated accordingly. Finally, by use of the patterns, no extra space is required for the marks and multiple windows can be used throughout the exposure site to improve the performance even further.

The proposed pattern-assisted algorithm can be summarized as follows (see also Figure 10):

1. Using global alignment to align the image of next layer to the previous one at a few check points

2. Estimating the distortion function over the entire substrate after processing each layer using the actual pattern on the substrate

3. Using the estimated distortion function to *interpolate* between alignment sites *i.e.* to predict the location of intermediate cells and compensate for the misalignment accordingly.

The pattern-assisted algorithm is based on computing the distortion using a reference image and a windowed image. The reference image depends on the mask and optical exposure system and is the image that will be viewed in the windowed image given there is no distortion in the wafer. The reference image can either be simulated by using an optical simulator to simulate the database image or can be extracted by careful adjustment of the wafer image for a specific exposure pattern. The reference image is then compared with the windowed image that is obtained by taking an image of the wafer pattern through an alignment window, as shown in the following diagram:

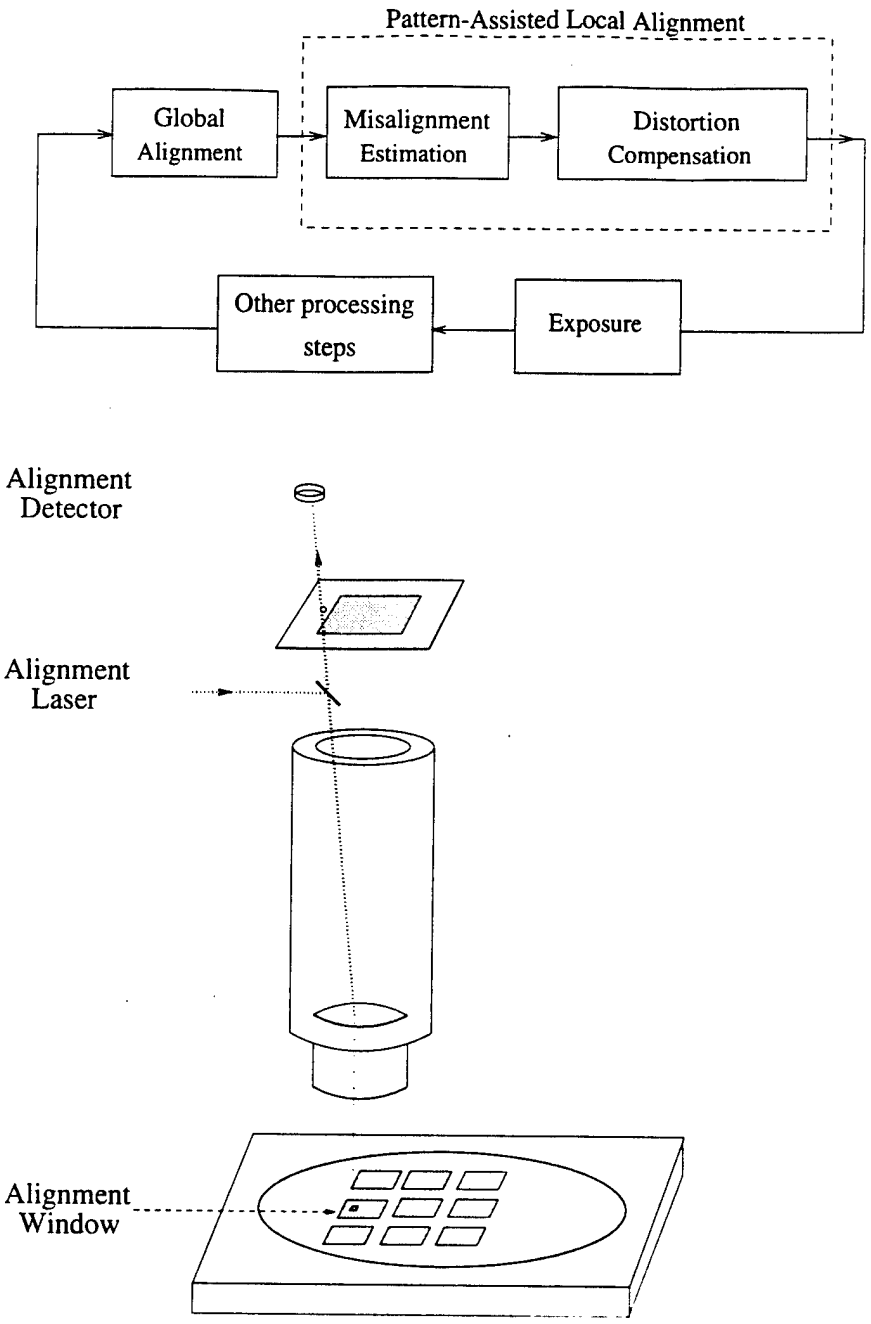

Figure 10: Schematic of pattern-assisted alignment scheme

$$\begin{array}{lcl} \text{Wafer} & \xrightarrow{\textit{Optical sensor}} & \text{Windowed Image} \\ \text{Mask} & \xrightarrow{\textit{Simulator}} & \text{Reference Database Image} \end{array}$$

After extraction of the reference and windowed images, the misadjustments between these images can be used for estimating the distortion pattern. The horizontal and vertical misalignment of the pattern in a reference window are estimated separately by projecting the two-dimensional pattern in the window in both directions. After using global alignment schemes at a few points to provide a reference for the whole wafer, the estimated misalignment is used to compensate for the existing distortion. The new mask is then exposed at the locations estimated by the distortion estimation algorithm. Figure 11(a) shows image of an original LCD pattern which is retrieved from a database and will be used as a reference. Due to distortion, this pattern is shifted in the reference window, and an image shown in Figure 11(b) is received through the window after the global alignment step.

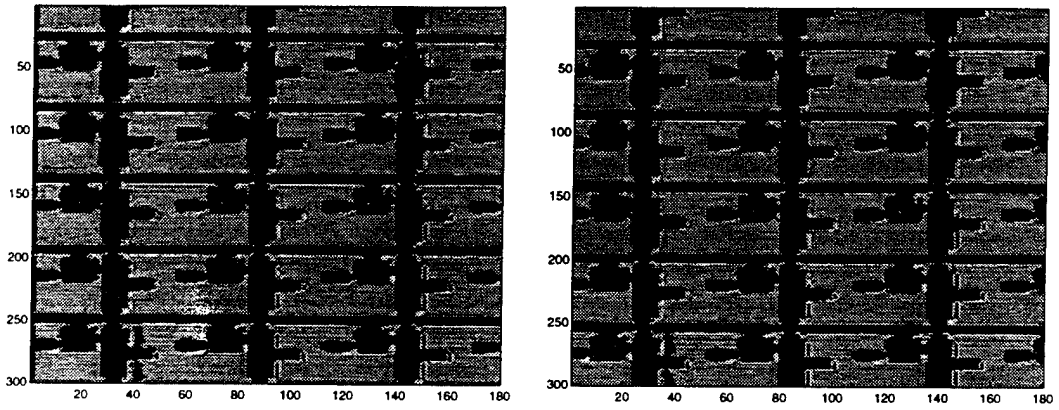

Figure 11: The original database image of the reference window (a) and shifted image of the reference window after introduction of distortion in the substrate (b)

By projecting the images of Figure 11 on the vertical axis, the projection vector $\mathbf{y}_{proj}$ contains the required information for estimating the vertical misalignment of cells in that image. In this way, the problem will be reduced to estimating the relative location of a specific pattern in a one-dimensional signal with respect to a reference signal. In this case the reference signal can be obtained by projecting the original image (Figure 11) in both directions. The general problem of localizing a pattern in a received signal arises in a wide range of applications such as in communications systems, radar and sonar signal processing, and geophysical data processing. The standard method for solving this problem is based on

autocorrelation techniques that can be computationally improved by FFT methods. After removing the bias of $\mathbf{y}_{proj}$ by subtracting its mean, the signal is correlated with the projected reference signal. The local maxima of the cross-correlation function give an estimate of δ_x and δ_y.

The results of estimating the amount of misalignment of each cell is examined for both the proposed method and the method that only uses global alignment at a few checkpoints. Figure 12 shows the performance of the two methods. As can be easily verified, the proposed method provides better accuracy than the case where only conventional alignment schemes are used.

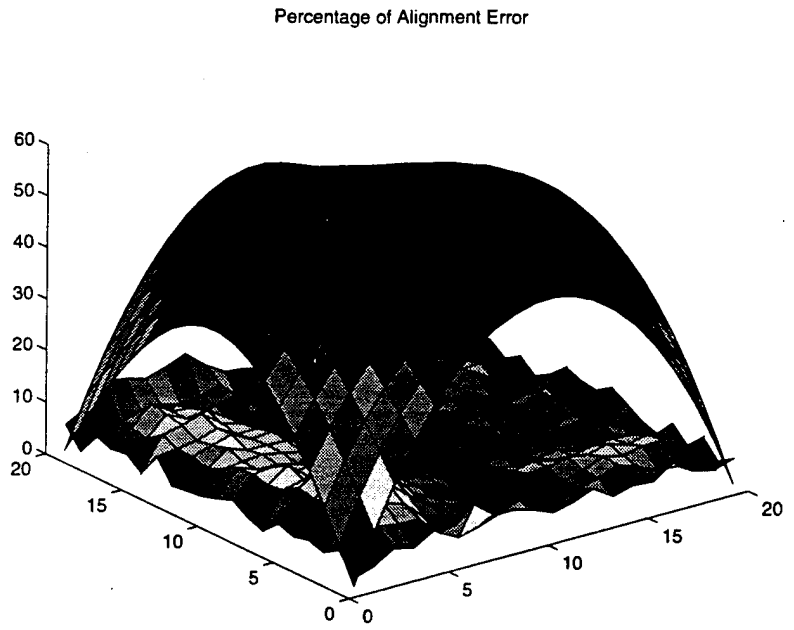

Figure 12: Misalignment error of cells in each window for two different schemes: Lower graph shows the error of the proposed scheme whereas the upper graph shows the error of using a four-point global alignment method

4.3 Future Research Possibilities

- Incorporating possible 2D models for nonlinear distortion
- Optimizing the location of alignment windows on the substrate
- Investigating the optimum choice of imaging procedure for acquiring the windowed image

- Investigating new schemes for improving the contrast of acquired images for comparison with database images

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5 Phase-Shifting Mask Design

The continuing effort to achieve higher density integrated circuits by fabricating circuits with smaller device sizes offers significant technological challenges to the IC manufacturing industry, and in particular to the microlithography community. Despite numerous predictions of its demise, optical lithography remains the the backbone of today's integrated circuit manufacturing industry. The prohibitive costs of retooling an entire fabrication line to accommodate nascent technologies such as X-ray lithography has further fueled a very aggressive effort to extend the capabilities of optical lithography to decrease device sizes.

The goals of our efforts in this area were to study the problem of efficient automated design of phase-shifting masks - one of the more promising candidate (*optical enhancement*) technologies for extending the capabilities of optical lithography. Other candidate enhancement technologies include modified illumination schemes, pupil filtering, and optical proximity correction (OPC).

Some specific accomplishments of this project were:

1. Development of a new and computationally efficient class of mathematical models describing partially coherent optical systems used for optical lithography.

2. Development of fast automated design algorithms for phase-shifting mask design.

3. A novel double exposure lithography technique for application with phase-shifting masks.

4. Development of a Fast Aerial Imaging Algorithm by exploiting coherent approximations and IC pattern structure.

Computationally Efficient Optical Projection Models

As a starting point for our investigation of automated PSM design algorithms, we examined the optical projection process. It was our intention to use a model-based approach to the design problem, and therefore a suitable model was necessary. We found however that existing models for partially coherent projection systems were too computationally inefficient for application to a realistic mask design setting.

The size of a typical integrated circuit is in the range of 100mm^2. Discretization of this area using a sufficiently fine sampling grid produces roughly $N = 10^{10}$ sample points. To compute the image of a mask this size using existing models for partially coherent imaging

would have required $\mathcal{O}(N^2) \approx 10^{20}$ operations, which translates to many years of computation on present day computers.

We showed that it is mathematically possible to construct a class of simple approximations to the partially coherent imaging system model. These approximate models, which are referred to as *Optimal Coherent Approximations* (OCA), reduced the computational complexity of the image simulation problem to $\mathcal{O}(N \log N) \approx 10^{11}$ operations. These results are described in [5].

We also showed analytically that for typical partially coherent projection systems used in optical lithography, the error introduced by such approximations is uniformly bounded and small.

In addition to the application in our work on phase-shifting mask design described below, the OCA class of optical system models was further utilized in developing a very fast and accurate aerial image simulation program that has recently received considerable attention from industry.

Automated Phase-Shifting Mask Design

The OCA imaging model was used as a basis for the development of a fast automated model-based PSM design algorithm. Taking a systems viewpoint, we formulated the problem of PSM design as a nonlinear inverse problem where the mask is regarded as the input to a projection system that produces an intensity image as its output. The goal of PSM design then becomes to systematically determine a phase-shifting mask design that, when applied to the projection system, produces an intensity image that is 'close' to the desired intensity image, which is determined from the circuit layout.

We showed that in the framework of OCA models, a key step in the solution of the PSM design problem could be reduced to the problem of *phase-retrieval* - a classical inverse problem in image processing and optics. This enabled us to develop an efficient derivative of the so-called Gerchberg-Saxton phase retrieval algorithm to help solve the PSM design problem for arbitrary layout patterns. Several other signal processing ideas [*esp.* bandlimited extrapolation and half-toning techniques (see sec. 5.2)] have been used to obtain a reasonably complete solution, which will be described in the Ph.D. thesis of Mr. Y. T. Wang. A Hewlett Packard Research Lab group is helping to actually fabricate some masks based on our methodology.

A key feature of this algorithm is that the computational effort required per iteration is $O(N \log N)$, where N is the number of discrete image points considered; this is significantly

less computation than is required for other model-based phase-shifting mask design algorithms proposed to date [4, 3, 2, 1]. The PSM design algorithm and some of the simulation and experimental results of this work are reported in [5, 6].

As a further illustration of the interdisciplinary flavor of our work, we note that these ideas also led to a new algorithm for separating constant-modulus signals impinging on an antenna array at the same carrier frequency, but from different directions [11].

5.1 Double-Exposure-Two-Phase (DETP) Masks

In our study of the manufacturability of masks designed by our automated algorithm, we also discovered a number of interesting theoretical results that seem to have significant practical implications. In particular, we showed that:

(i) Phase shifting masks to achieve any desired Manhattan wafer pattern can be obtained using no more than 4 distinct phases; moreover there exist layouts that will require 4 phases.

(ii) (Double-Exposure Theorem) Every focal plane image that may be achieved using a single phase-shifting mask with *continuously varying* phase, may also be achieved using a suitably selected *pair* of two-phase masks *i.e.* masks with only 0° and 180° phase.

The Double Exposure theorem was a somewhat surprising result that was derived using the OCA model formulation as a tool, and it motivated us to begin exploring an alternative PSM strategy that involves two successive exposures and employs a pair of two-phase masks. Two important benefits are derived from application of the Double-Exposure Theorem; they are:

(i) Quantization of the phase values on the mask to meet manufacturing capabilities is completely unnecessary since each mask requires only a single phase-shift value of 180°.

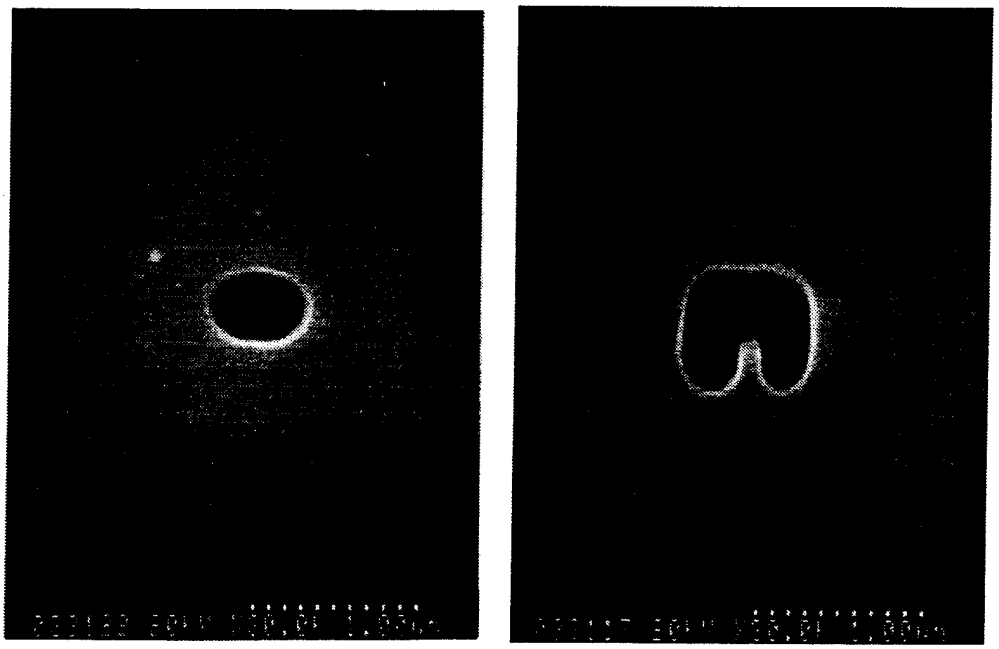
(ii) The integrity of the image under defocus conditions is preserved better than that of an image generated by a single phase-shifting mask with more than two phase values.

A detailed description of these results may be found in the papers [5, 6, 10].

Experimental Testing of Double Mask System

In the early part of 1994, we completed an initial set of experimental trials of our design algorithm and the double-exposure PSM method. This experimental work was made possible

through a collaborative effort with Mr. Hisashi Watanabe of Matsushita Corporation, Japan, who was at the time visiting with Professor Fabian Pease's group at Stanford. We tested a number of simple patterns such as contact holes, gratings, and U-patterns, with features sizes ranging from 0.25μm to 0.35μm. We also tested a number of more complicated designs, including a SRAM design and a gate array design, that were aimed at demonstrating the benefits of using two DETP masks. Experimental results for a 0.25μm U-pattern are shown in Fig. 13. These experiments were all performed using a I-line (365nm wavelength) projection printer with a numerical aperture of 0.57; the Rayleigh resolution limit for this system is about 0.38μm. Note that the pattern is completely undefined using a conventional transmission mask, while we get very good pattern definition with the double-exposure PSM's. These initial results were encouraging, and even more so due to the fact that they



(a) (b)

Figure 13: (a): SEM micrograph of the resist U-Pattern exposed using a conventional transmission mask. **(b)**: SEM micrograph of the resist U-Pattern using the designed double-exposure PSM's. The target feature size is 0.25μm. The Rayleigh limit for the optical system is 0.38μm.

were successful on the first attempt. One possible criticism of the double-exposure scheme is that the alignment requirements of the second exposure step may adversely affect both throughput and yield. Mr. Watanabe demonstrated that by placing the pair of masks on the same physical reticle, the alignment of the second exposure can be handled by a precise

translation of the wafer stage, so that neither yield nor throughput are serious limitations on this approach.

For more complicated patterns, our experimental work focused on demonstrating the enhancement of depth-of-focus using DETP masks. This enhancement in depth-of-focus is illustrated by the example shown in Fig. 5.1. The figure shows SEM micrographs of patterned resist using both the double-exposure-two-phase (DETP) masks and a conventional mask. The feature size is 0.35μm, and the experiments were performed using a $I - line$ (365nm) stepper with a numerical aperture of $NA = 0.57$. The improvement obtained using the DETP masks is quite clear from the defocussed images.

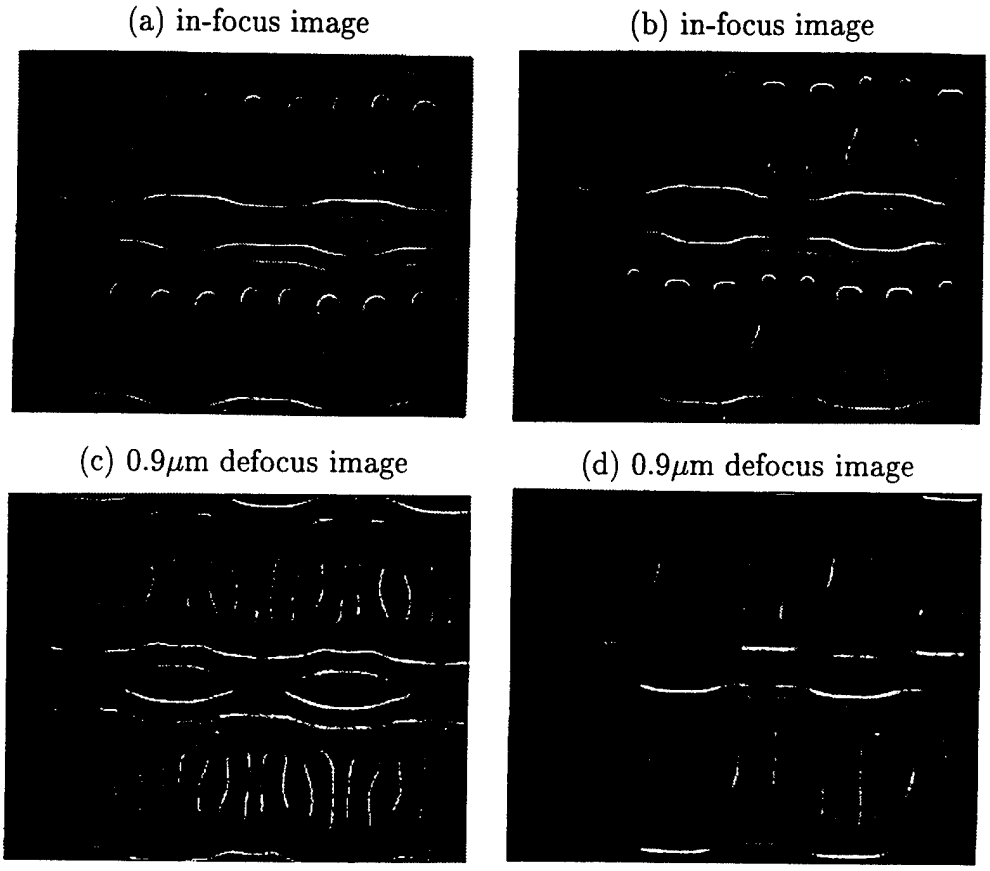


Figure 14: (b) & (d): SEM images of SRAM by DETP masks PSM, (a) & (c): SEM images using conventional mask

The enhanced depth-of-focus was also verified experimentally for the Nikon Maze pattern along with the SRAM and gate array patterns. The results of this initial set of of experimental work are described in detail in the paper [8].

5.2 Fast Aerial Image Computation

Modeling aerial images has recently become a crucial component of semiconductor manufacturing. As all steppers employ partially coherent illumination, such modeling has been computationally intensive for all but elementary patterns. We have developed a fast computational method for calculating aerial images of integrated circuit masks produced by a partially coherent optical projection system. The method described relies on two tools to realize fast computation: (i) Coherent decomposisitions of partially coherent imaging system models as proposed by Pati and Kailath [5], and (ii) The use of 'basis' (or building block) images that are well-suited to describe integrated circuit patterns. Several examples have been run in which aerial images are speedily computed for large mask areas. The proposed method represents a speed improvement of several orders of magnitude over a more traditional, and more general, approach (SPLAT from U.C. Berkeley). A paper on this has been submitted to the IEEE Transactions on Semiconductor Manufacturing [9].

5.3 Work in Progress and Future Directions

As a result of simulation trials on more complicated layout patterns we determined that simple threshold quantization of mask transmittance, as used in our prior work and experiments, is inadequate. This has led to the novel concept of using a form of halftoning to design masks that approximate the performance of masks with continuously-varying transmittance. This requires that relatively small features be precisely fabricated on the mask, and the idea was initially met with some skepticism from industry regarding the manufacturability of such halftoned masks. However, through collaboration with the Advanced Lithography Group of HP ULSI Research Laboratory in Palo Alto, a first experimental trial of these halftoning ideas is nearing completion. It has been shown that such masks can indeed be fabricated. We are hoping to obtain the final results of these trials soon. Figure 15 shows some of the early experimental halftone masks obtained.

In addition, at least one other major manufacturer has shown considerable interest in exploring the idea of double-exposure and halftoned phase-shifting masks, and our own work on the techniques is continuing.

A software package, which includes an interface to standard integrated circuit CAD tools, is now largely complete. This software package serves to integrate many of the results and algorithms that we have developed into a single environment. It is also serving as a useful tool for further research.

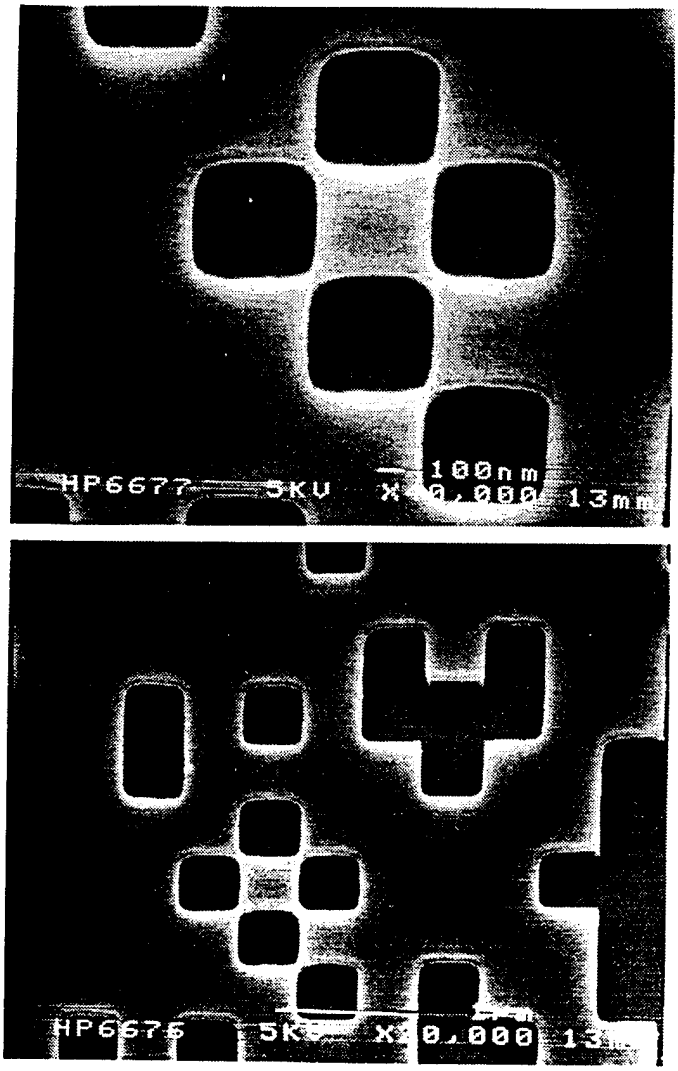


Figure 15: SEM micrographs of halftoned masks made at HP ULSI Research Laboratories, Palo Alto, CA.

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6 Related Research

6.1 Modeling of Rapid Thermal Chemical Vapor Deposition

A radiant heat transfer model was verified for a susceptor-less multizone rapid thermal chemical vapor deposition (RTCVD) system. Qualitative agreement was shown between thermal model predictions and temperature measurements as deduced via experimental film thickness measurements of polysilicon. The analysis was used to demonstrate that a wafer support mechanism overlapping the edge of the wafer in an RTCVD system contributes significantly to spatial nonuniformities and nonsymmetries. The thermal model was also verified by demonstrating qualitative agreement between the lamp powers predicted by the model to be the optimal settings with those that were determined experimentally to be approximately the optimal settings. In addition, the applicability of the model was also studied by examining the performance of a closed-loop temperature controller designed using the model. The model-based controller was demonstrated to produce better repeatable film thicknesses than an open-loop method through comparative experimental studies of 24 consecutively processed wafers.

6.2 Improvements in C_{pk} using real-time feedback control

The usual approach to bring the value of the process capability index, C_{pk}, to an acceptable level is to design equipment and develop a process in which the process variable is robust to external disturbances. However, an alternative approach involves the use of *in-situ* sensors and real-time feedback control. Currently this approach is not widely implemented in the semiconductor industry. In this work we provided analytic justification to quantify the potential improvement in C_{pk} if a real-time feedback control scheme is used instead of the usual open-loop approach. We showed that for the case of feedback control the level of C_{pk} is only limited by the accuracy and reproducibility of the sensor provided that the target values were indeed achievable by the processing equipment. This result also held in the presence of disturbances and nonlinearities. C_{pk} values for open-loop and real-time feedback control strategies were compared for two experimental applications: single-wafer CVD nitride and polysilicon processes.

6.3 Computational Methods

We also continued to pursue in a small way further development of the fast estimation, identification and control algorithms useful in manufacturing applications. These include work on new classes of convex optimization algorithms, adaptive filtering and smoothing algorithms.

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Appendix A - IEEE TSM 1993 Best Paper Award

Best Paper Award

THE IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING Best Paper Award is presented to the authors of that paper considered by the TRANSACTIONS' Editorial Staff and reviewers to be the most outstanding paper published during the year. The Award is based on the accuracy, originality, and importance of the technical concept, as well as the quality and readability of the manuscript.

The Award will be presented at the ASMC in the Boston area this Fall.

We are pleased to announce that the paper entitled "Model Identification in Rapid Thermal Processing Systems" by Y. M. Cho and T. Kailath has been recognized as the best paper published in the TRANSACTIONS in 1993. This paper, that appeared in the August issue, has been chosen because it represents one of the first successful attempts to mate formal control theory with an important, practical problem in semiconductor processing. We anticipate that this work will open the way to solving many more real-time control problems in future IC production.

COSTAS J. SPANOS AND GARY CHEEK
Editors

Thomas Kailath (S'57–M'62–F'70) was educated in Poona, India, and received S.M. and Sc.D. degrees from the Massachusetts Institute of Technology in 1959 and 1961, respectively.

From October 1961 to December 1962 he worked at the Jet Propulsion Laboratories, Pasadena, CA, where he also taught part-time at the California Institute of Technology. He then came to Stanford University, where he served as Director of the Information Systems Laboratory from 1971 through 1980, as Associate Department Chairman from 1981 to 1987, and currently holds the Hitachi America Professorship in Engineering. He has held short term appointments at several institutions around the world. Dr. Kailath has worked in a number of areas including information theory, communications, computation, control, signal processing, VLSI design, statistics, linear algebra and operator theory; his recent interests include applications of signal processing, computation and control to problems in semiconductor manufacturing and wireless communications. He is the author of *Linear Systems*, Prentice Hall, 1980, and *Lectures on Wiener and Kalman Filtering*, Springer-Verlag, 1981. He has held Guggenheim, Churchill and Royal Society fellowships, among others, and received awards from the IEEE Information Theory Society and the American Control Council, in addition to the Technical Achievement and Society Awards of the IEEE Signal Processing Society. He served as President of the IEEE Information Theory Society in 1975, and has been awarded honorary doctorates by Linköping University, Sweden, and by Strathclyde University, Scotland.

Dr. Kailath is a Fellow of the IEEE and of the Institute of Mathematical Statistics and is a member of the National Academy of Engineering and the American Academy of Arts and Sciences.

Young Man Cho received the B.S. degree in control instrumentation engineering from Seoul National University in Korea, in 1989 and the M.S., Ph.D. in electrical engineering from Stanford University, Stanford, CA in 1991 and 1993, respectively.

From 1993 to April 1994, he has worked as a Post-Doctoral research fellow in electrical engineering at Stanford University, in the area of system identification and its application to semiconductor manufacturing. He is currently working as an associate scientist at United Techology research center, East Hartford, CT. He has worked in several areas including system identification and its application to semiconductor manufacturing with an emphasis on temperature control and measurement in rapid thermal processing, numerical linear algebra and signal processing. His current research interests are in temperature estimation and lamp array design in rapid thermal processing.

Notice of 1993 Best Paper Award from the *IEEE Transactions on Semiconductor Manufacturing*

Appendix B - Abstracts of Completed Ph.D. Theses

Fast Subspace Based System Identification: Theory and Practice - Young Man Cho (Dec. 1993)

System identification techniques have been extensively studied for several decades. However, most of the available methods are proposed for scalar (SISO) systems described by high-order input-output models (ARMA or ARMAX). Until recently, however, the identification of state-space models has attracted much less attention. This recent surge of interest stems from some unique advantages of state space identification over input-output (I/O) based identification: better numerical conditioning, the ability to estimate of the number of states (or the model order), simple extensions to multi-input, multi-output (MIMO) systems.

The main drawbacks of direct state-space identification techniques are the high computation and storage costs. For example, the subspace identification algorithm of De Moor *et al.* involves a singular value decomposition and an eigendecomposition, which require $O(MN^2 + M^2N + M^3)$ flops and $O(MN + M^2 + N^2)$ storage, where N is the data length and M is a so-called sliding window size. When $N = 1000$ and $M = 100$ as could often be the case, the associated process ran for approximately one hour and storage grew to 100 Mbytes, on an otherwise unloaded SUN 4/370 with a MATLAB implementation of the algorithm. In this talk, we propose a state-space identification method that leads to orders-of-magnitude reduction in both computation time and storage. Such time and storage savings are achieved by exploiting the Hankel (or Toeplitz) structure of the data matrix, and the low-rank + shift ($\sigma^2\mathbf{I}$) structure of the covariance matrix. Displacement structure theory and the recently developed FSD (fast subspace decomposition) method are two main vehicles that make the fast implementation possible. As a result, our method requires only $O(MN)$ flops and $O(N + M^2)$ storage space. For the same example given earlier (*i.e.*, $N = 1000$ and $M = 100$), the fast implementation took only several seconds and required less than 1 Mbytes.

The methods proposed here are illustrated via an application to the identification of a real system, *i.e.*, a rapid thermal processor (RTP) for semiconductor manufacturing to test the viability of the new identification technique. After a brief description of RTP, the identification procedure will be discussed including input design, data acquisition, data processing, and model validation. We also show results of control experiments based on a model identified by the proposed technique.

Broadband Switching:Architectural Design, Performance Analysis, and Applications - Chih-Yuan Chang (Dec. 1994)

Broadband integrated services digital networks (B-ISDN) are envisioned to be the universal communications framework, integrating not only all existing services but also new services yet to be imagined. Asynchronous transfer mode (ATM) has been selected as the transmission and switching technique for use in B-ISDN. It promises to handle all kinds of information (*e.g.* , audio, video, text, image, data, etc.) in an integrated manner. Moreover, ATM provides a very fine bandwidth granularity and hence can be used efficiently in applications ranging from low-speed voice service to high-speed video communication. the desktop workstations demand for an expanding diversity of services in the broadband network, efficient ATM switch architectures are becoming increasingly desirable.

Switch architectures based on Batcher-banyan networks are considered the most suitable for constructing large-dimension ATM switches. Though the Batcher-banyan network is internally nonblocking, the ubiquitous problem of packet loss resulting from output conflict can only be reduced by buffering. Buffering strategies are basically categorized into two classes: input buffering and output buffering. For input-buffered switches, a phenomenon called head-of-the-line (HOL) blocking limits the maximum throughput to only 58.6 percent $(2 - \sqrt{2})$. On the other hand, output buffering achieves much higher throughput, but the entire switch has to be operated at a sufficiently high speed in order to deliver all the packets simultaneously destined for the same outlet. This generally imposes severe implementation problems.

We propose a switch architecture with combined input and output queuing. The switch fabric consists of a Batcher sorting network, a radix-r shuffle mapping network, and r parallel distributing modules. The input queues and the switch fabric run at the same speed as the input and output trunks, whereas the speed of the output queues is increased by a factor of r.

We analyze the throughput-delay characteristics of the proposed switch. The maximum throughput in the case where $r = 2$ is 88.6 percent. For $r = 4$, the proposed switch offers a 99.6 percent maximum throughput. In addition, the proposed switch relieves the HOL blocking by allowing up to r packets to be delivered to the same outlet in one time slot. Consequently, the average delay is also reduced. The above results suggest that a moderate speedup at the output queues is sufficient to achieve high performance.

We also present a simple application of the proposed switch to ATM local area networks (LAN). In a LAN environment, achieving high link utilization is not a major considera-

tion. Instead, understanding the traffic characteristics and ensuring the quality of service are the primary issues. Based on our performance analysis and the self-similar characteristics of TCP/IP traffic, we propose a new quality of service provision policy from a switch perspective.

ATM networks are designed to provide a ubiquitous infrastructure for multiservice unification. Its operating environments can vary from backbone wide area networks to wireless local area networks. For applying ATM in a wireless local area network where the physical medium is always shared, admission control for the shared spectrum is an important consideration. Hence, we study an admission control technique for applying ATM in a wireless local area network.

Convex Optimization Techniques in Control and Estimation - Pooyeon Park (Aug. 1995)

Several analysis and synthesis problems in system theory can be reduced to problems of solving first- or second-order matrix polynomial equations, such as Lyapunov equations (LEs) or algebraic Riccati equations (AREs). By now, various methods are available for solving such equations, *e.g.*, Newton iterations, invariant subspace methods using Hamiltonian matrices, generalized eigenvalue methods, and matrix-sign-function methods. However, when the problems have additional constraints, or unknowns other than the LE and ARE variables, one can rarely solve them by reduction to LEs or AREs.

It has been emphasized that many problems arising in system theory can be cast into the form of first-order matrix polynomial inequalities called linear matrix inequalities (LMIs), which belong to the group of convex problems and thus one can not only efficiently find feasible and global solutions to them via interior-point methods, but can also easily handle many additional linear equality or inequality constraints and unknowns.

In this thesis, we present one useful technique for reformulating such problems into LMI problems, by introducing the concepts of Popov functions and dual or complementary Popov functions and the generalized KYP lemma. The most significant observation is that if either the Popov function or the dual Popov function is semidefinite, we can readily obtain an LMI and thus solve the problem via (linear) convex programming.

Using this technique, we provide a new solution to the so-called dual $\mathcal{J}$-spectral factorization and reformulate a level-γ $\mathcal{H}_\infty$ filtering problem into an LMI problem so as to handle the *optimal* $\mathcal{H}_\infty$ filtering problem, too.

To illustrate the advantages of such formulations, several control problems are considered

in uncertain linear systems with norm-bounded feedback restriction: a stability analysis problem, an output-feedback stabilizer design problem, the *optimal* guaranteed cost LQR problem, and the *optimal* guaranteed-γ $\mathcal{H}_\infty$ control problem. Such problems usually require additional variables beyond an ARE variable in order to deal with uncertainties. Therefore, LMI, rather than ARE, formulations allow us to find their solutions.

Modern Signal Processing Techniques for IC Inspection and Lithographic Alignment - Babak Khalaj (June, 1996)

As the complexity of integrated circuits is increasing rapidly, the need for faster, more reliable and more accurate techniques becomes even more important for maintaining high throughput and high yield in the fabrication process. In this dissertation, we will present applications of modern signal processing techniques to the fields of automatic defect inspection of periodic patterns and lithographic alignment. The inspection and alignment steps have a crucial impact on the yield and throughput of the overall process, regardless of the specific lithographic scheme used (optical, x-ray, etc.)

The task of detection and localization of defects in VLSI wafers and masks can be expensive and exhausting. The algorithms that are currently used for inspection of images with repeating structures require sophisticated hardware or manual scaling to match the periods of their acquired images to their prior period estimates. Our proposed approach assumes no prior knowledge about the repetition periods and uses high resolution spectral estimation techniques to reduce the sensitivity of the inspection process to scaling errors. Potential applications of the proposed algorithm range from the problem of wafer and mask defect inspection of memory chips to problems such as the inspection of flat panel displays and CCD arrays.

In general, repeated patterns are shifted from their desired position on a rectangular grid because of thermal effects, flexibility of large substrates, and lithographic imperfections. As feature sizes get smaller, in order to produce a defect-free reference image and locate the defective cells, it becomes necessary to estimate the misalignment of each cell beforehand. The existing distortion in the substrate is estimated by applying recently-developed projection-based ideas that we use to obtain low computational complexity schemes.

We shall also study the application of methods developed for estimating substrate distortion to the problem of lithographic alignment of patterned substrates with low-order distortions. At every step of the lithography process, new mask patterns must be accurately aligned with previous patterns on the wafer surface. Site-by-site or local alignment

requires aligning the mask to the wafer at each exposure; global alignment on the other hand is carried out by aligning at a few sites throughout the wafer and then stepping the stage to estimated locations. While avoiding time-consuming alignment procedures, the proposed techniques will improve the performance of alignment schemes by estimating the process-induced distortion in the substrate.